

## Content

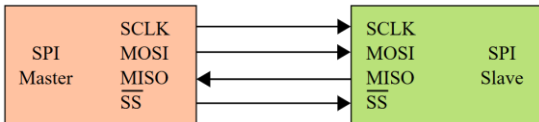
1.	SPI Protocol	1
1.1	Bus Topology	1
1.2	Electrical Characteristics	2
1.3	SPI Mode	2
1.4	MOSI (Master Out, Slave In)	2
1.5	MISO (Master In, Slave Out)	2
1.6	/SS Slave Select	2
1.7	Master Start-up	2
1.8	Slave Start-up	2
1.9	Timing	3
1.10	Slave Reset	3
1.11	Frame Layer	3
1.12	Data Frame Structure	4
1.13	Timing	4
1.14	Data Structure	4
1.15	Angle Calculation	4
1.16	Error Handling	4
1.17	Document Changes	4

## 1. SPI Protocol

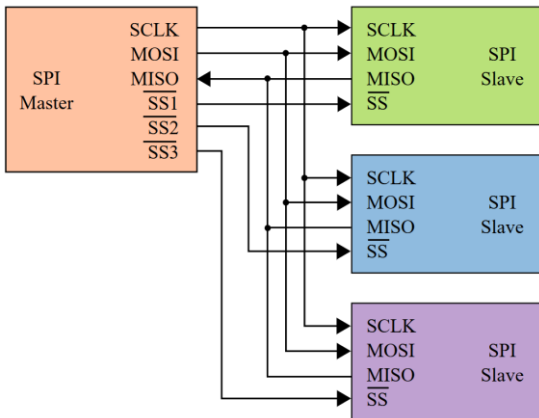
This document reflects the Novotechnik sensor protocol implementation of the standard SPI protocol. A basic knowledge of the SPI Bus is required for a proper understanding of this document.

### 1.1 Bus Topology

SPI communication with only 1 slave:



SPI communication with more than 1 slave:

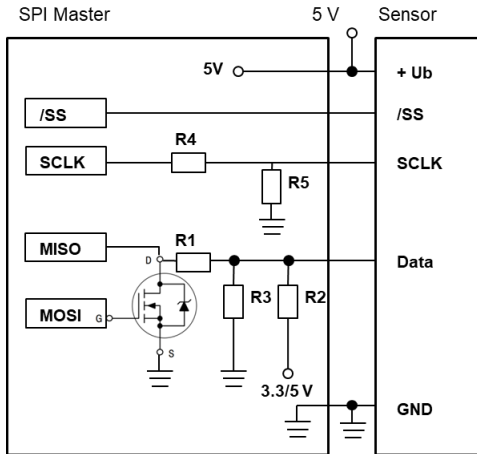


**1.2 Electrical Characteristics**

The serial protocol of Novotechnik Single turn sensors is a three wires protocol (/SS, SCLK, MOSI-MISO).

The rotary sensor is considered as a slave mode:

- /SS pin is a 5V tolerant digital input
- SCLK pin is a 5V tolerant digital input
- MOSI-MISO pin (both lines are combined in the sensor to form one data line) is a 5V tolerant open drain digital input/output



Resistor values

Application type	µCtrl supply [V]	Pull-up supply [V]	Sensor supply [V]	R1 [Ω]	R2 [Ω]	R3 [Ω]	R4 [Ω]	R5 [Ω]	MOS type
5 V µCtrl w/o O.D. w/o 3.3 V	5 V	5 V	5 V	100	1000	20000	1000	20000	BS 170
5 V µCtrl w/o O.D. w 3.3 V	5 V	3.3 V	5 V	150	1000	-	1000	20000	BS 170
3.3 V µCtrl w/o O.D. *	3.3 V	3.3 V	5 V	150	1000	-	-	-	BS 170
5 V µCtrl w O.D. w/o 3.3 V**	5 V	5 V	5 V	100	1000	20000	1000	20000	-
3.3 V µCtrl w O.D.	3.3 V	3.3 V	5 V	150	1000	-	-	-	-

\*) µCtrl w O.D.: Micro Controller with open-drain capability (e.g. NEC V850 series)

\*\*) µCtrl w/o O.D.: Micro Controller without open-drain capability (e.g. TI TMS320 series, AMTEL AVR)

**1.3 SPI Mode**

Clock phase CPHA = 1 even clock changes are used to sample the data

Clock polarity CPOL = 0 active high clock

The positive going edge shifts a bit to the slave's output stage and the negative going edge samples the bit at the master's input stage.

**1.4 MOSI (Master Out, Slave In)**

The master sends a command to the slave to get the angle information.

**1.5 MISO (Master In, Slave Out)**

The MISO of the slave is an open-collector stage. Due to the capacitive load a > 1k Ohmpull-up is used for the recessive high level.

**1.6 /SS Slave Select**

The /SS pin enables a frame transfer (if CPHA = 1). It allows a re-synchronisation between slave and master in case of communication error.

**1.7 Master Start-up**

/SS, SCLK, MISO can be undefined during the master start-up as long as the slave is re-synchronized before the first frame transfer.

**1.8 Slave Start-up**

The slave start-up (after power-up or an internal failure) takes 10 ms. Within this time /SS and SCLK is ignored by the slave. The first frame can therefore be sent after 10 ms.

MISO is high-impedant until the slave is selected by its /SS input.

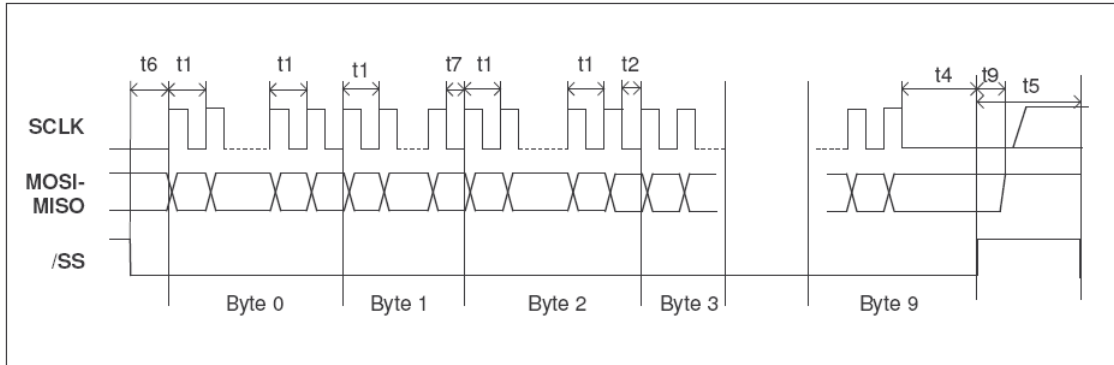
The sensor will cope with any signal from the master while starting up.

**1.9 Timing**

To synchronize communication, the master deactivates /SS high for at least t5 (300 µs). In this case, the slave will be ready to receive a new frame.

The master can re-synchronize at any time, even in the middle of a byte transfer.

Note: Any time shorter than t5 leads to an undefined frame state, because slave may or may not have seen /SS inactive.



Timing	Min	Max	Remarks
t1	2.3 µs	-	No capacitive load on MISO. t1 is the minimum clock period for any bits within a byte
t2	12.5 µs	-	t2 is the minimum time between any other byte
t4	2.3 µs	-	Time between last clock and /SS = high
t5	300 µs	-	Minimum /SS = high time where it is guaranteed that a frame re-entrance will be started
t5	0 µs	-	Minimum /SS = high time where it is guaranteed that <u>no</u> frame re-entrance will be started
t6	2.3 µs	-	Time t6 defines the minimum time between /SS = low and the first clock edge
t7	15 µs	-	t7 is the minimum time between start byte and byte 0
t8	0µs	-	Minimum time where SS is deactivated between an ID byte and a start byte
t9	-	<1 µs	Maximum time between /SS = high and MISO Bus High-Impedance
t start up	-	<10 ms	

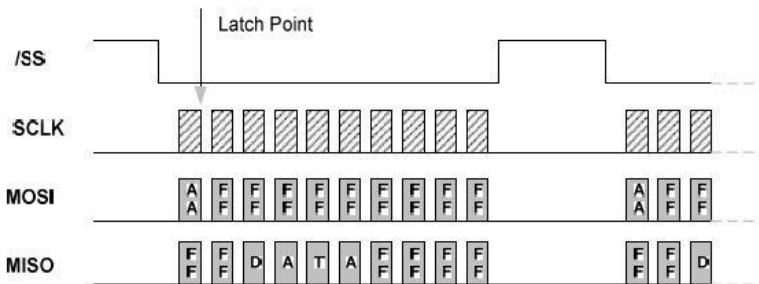
**1.10 Slave Reset**

On internal soft failures the slave will reset after 1 s, or after an (error) frame is sent. On internal hard failures the slave will reset itself. In that case the serial protocol will not come up. The serial protocol link is enable only after the completion of the first synchronisation (the master deactivates /SS for at least t5).

**1.11 Frame Layer**

Before each transmission of a data frame, the master should send a byte AAh to enable a frame transfer.

The latch point for the angle measurement is at the last clock of the first data frame byte.



Timing diagram - dual slave communication

**1.12 Data Frame Structure**

A data frame consists of 10 bytes

- 2 start bytes (AAh followed by FFh)
- 2 data bytes (Data 16 – most significant byte first)
- 2 inverted data bytes (/Data16 - most significant byte first)
- 4 all-high bytes

The master should send AAh followed by nine bytes FFh.

The slave will answer with two bytes FFh followed by four data bytes and four bytes FFh.

**1.13 Timing**

There are no timing limits for frames: a frame transmission could be initiated at any time.

There is no inter-frame time defined.

**1.14 Data Structure**

The Data16 could be a valid angle or an error condition. The two meanings are distinguished by the LSB.

Data 16: Angle A [13:0] with (Angle Span) /2^14

Most Significant Byte								Less Significant Byte							
MSB							LSB	MSB							LSB
A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	0	1

Data 16: Error

Most Significant Byte								Less Significant Byte							
MSB							LSB	MSB							LSB
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

BIT	NAME	
E0	0	
E1	1	
E2	F_ADCMONITOR	ADC Failure
E3	F_ADCSATURA	ADC Saturation (Electrical failure or field too strong)
E4	F_RGTOOLOW	Analog gain below trimmed threshold (likely reason: field too weak)
E5	F_MAGTOOLOW	Magnetic field too weak
E6	F_MAGTOOHIGH	Magnetic field too strong
E7	F_RGTOOHIGH	Analog gain above trimmed threshold (likely reason: field too strong)
E8	F_FGCLAMP	Never occuring in serial protocol
E9	F_ROCLAMP	Analog chain rough offset compensation:clipping
E10	F_MT7V	Device supply VDD greater than 7V
E11	-	
E12	-	
E13	-	
E14	F_DACMONITOR	Never occuring in serial protocol
E15	-	

**1.15 Angle Calculation**

All communication timing is independent (asynchronous) of the angle data processing.

The angle is calculated continuously by the slave every 350 µs.

The last angle calculated is hold to be read by the master at any time.

**Note:** Only valid angles are transferred by the slave, because any internal failure of the slave will lead to a soft reset.

**1.16 Error Handling**

In case of any errors listed in chapter 1.12, the serial protocol will be initialized and the error condition can be read by the master. The slave will perform a soft reset once the error frame is sent.

In case of any other errors (ROM CRC error, EEPROM CRC error, RAM check error, intelligent watchdog error,...) the slave’s serial protocol is not initialized. The MOSI/MISO pin will stay high impedant (no error frame is sent).

**1.17 Document Changes**

Revision	Changes	Date	Who
V00	First edition	23.04.19	VM/mm
V01	1.2 Resistor value R3 and R5: 20000 Ohm instead of 20 Ohm	02.12.20	VM/mm